IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: TRAN-P059

#11 pay 326 of

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Serial No.: 09/694,433

Title: STATIC POWER CONTROL

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
5,201,059	METHOD FOR REDUCING POWER CONSUMPTION INCLUDES COMPARING VARIANCE IN NUMBER OF TIME MICROPROCESSOR TRIED TO REACT INPUT IN PREDEFINED PERIOD TO PREDEFINED VARIANCE	04/06/93
5,230,055	BATTERY OPERATED COMPUTER OPERATION SUSPENSION IN RESPONSE TO ENVIRONMENTAL SENSOR INPUTS	07/20/93
5,752,011	METHOD AND SYSTEM FOR CONTROLLING A PROCESSOR'S CLOCK FREQUENCY IN ACCORDANCE WITH THE PROCESSOR'S TEMPERATURE	05/12/98
6,216,235	THERMAL AND POWER MANAGEMENT FOR COMPUTER SYSTEMS	04/10/01
5,167,024	POWER MANAGEMENT FOR A LAPTOP COMPUTER WITH SLOW AND SLEEP MODES	11/24/92
5,218,704	REAL-TIME POWER CONSERVATION FOR PORTABLE COMPUTERS	06/08/93
5,239,652	ARRANGMENT FOR REDUCING COMPUTER POWER CONSUMPTION BY TURNING OFF THE MICROPROCESSOR WHEN INACTIVE	08/24/93
5,682,093	APPARATUS AND METHOD FOR REDUCING THE POWER CONSUMPTION OF AN ELECTRONIC DEVICE	10/28/97
5,717,319	METHOD TO REDUCE THE POWER CONSUMPTION OF AN ELECTRONIC DEVICE COMPRISING A VOLTAGE REGULATOR	02/10/98
5,086,501	COMPUTING SYSTEM WITH SELECTIVE OPERATING VOLTAGE AND BUS SPEED	02/04/92
6,157,092	METHOD AND CIRCUIT CONFIGURATION FOR VOLTAGE SUPPLY IN ELECTRIC FUNCTION UNITS	12/05/00
5,222,239	PROCESS AND APPARATUS FOR REDUCING POWER USAGE MICRO-PROCESSOR DEVICES OPERATING FROM STORED ENERGY SOURCES	06/22/93
5,726,901	SYSTEM FOR REPORTING COMPUTER ENERGY CONSUMPTION	03/10/98
5,812,860	METHOD AND APPARATUS PROVIDING MULTIPLE VOLTAGES AND FREQUENCIES SELECTABLE BASED ON REAL TIME CRITERIA TO CONTROL POWER CONSUMPTION	09/22/98

5,940,785	PERFORMANCE-TEMPERATURE OPTIMIZATION BY COOPERATIVELY VARYING THE VOLTAGE AND FREQUENCY OF A CIRCUIT	08/17/99
6,510,525	METHOD AND APPARATUS TO POWER UP AN INTEGRATED DEVICE FROM A LOW POWER STATE	01/21/03
6,457,135	SYSTEM AND METHOD FOR MANAGING A PLURALITY OF PROCESSOR PERFORMANCE STATES	09/24/02
6,388,432	CPU CORE VOLTAGE SWITCHING CIRCUIT	05/14/02
6,347,379	REDUCING POWER CONSUMPTION OF AN ELECTRONIC DEVICE	02/12/02
6,345,363	MICROPROCESSOR CORE POWER REDUCTION BY NOT RELOADING EXISTING OPERANDS	02/05/02
6,078,319	PROGRAMMABLE COREVOLTAGE SOLUTION FOR A VIDEO CONTROLLER	06/20/00
5,511,203	POWER MANAGEMENT SYSTEM DISTINGUISHING BETWEEN PRIMARY AND SECONDARY SYSTEM ACTIVITY	04/23/96
5,914,996	MULTIPLE CLOCK FREQUENCY DIVIDER WIITH FIFTY PERCENT DUTY CYCLE OUTPUT	06/22/99
5,774,703	DATA PROCESSING SYSTEM HAVING A REGISTER CONTROLLABLE SPEED	06/30/98
6,112,164	COMPUTER SYSTEM THERMAL MANAGEMENT	08/29/00
6,021,500	PROCESSOR WITH SLEEP AND DEEP SLEEP MODES	02/01/00
6,094,367	VOLTAGE REGULATING DEVICE FOR DYNAMICALLY REGULATING VOLTAGE IN A COMPUTER SYSTEM	07/25/00
5,630,110	METHOD AND APPARATUS FOR ENHANCING PERFORMANCE OF A PROCESSOR	05/13/97
5,687,114	INTEGRATED CIRCUIT FOR STORAGE AND RETRIEVAL OF MULTIPLE DIGITAL BITS PER NONVOLATILE MEMORY CELL	11/11/97
5,713,030	THERMAL MANAGEMENT DEVICE AND METHOD FOR A COMPUTER PROCESSOR	01/27/98
5,572,719	CLOCK CONTROL SYSTEM FOR MICROPROCESSOR INCLUDING A DELAY SENSING CIRCUIT	11/05/96
5,832,284	SELF REGULATING TEMPERATURE/PERFORMANCE/VOLTAGE SCHEME FOR MICROS (X86)	11/03/98
5,628,001	POWER SAVING METHOD AND APPARATUS FOR CHANGING THE FREQUENCY OF A CLOCK IN RESPONSE TO A START SIGNAL	05/06/97
5,710,929	MULTI-STATE POWER MANAGEMENT FOR COMPUTER SYSTEMS	01/20/98
5,913,067	APPARATUS FOR DAPTOVE POWER MANAGEMENT OF A COMPUTER SYSTEM	06/15/99
5,701,783	SETTING ANGLE ADJUSTER FOR THE CAR HEADLAMP	12/30/97
5,745,375	APPARATUS AND METHOD FOR CONTROLLING POWER USAGE	04/28/98

The Examiner's attention is respectfully directed to the following Published Patent Applications:

Pub No.	Title	Publication Date
2002/0026597	REDUCING LEAKAGE POWER CONSUMPTION	10/18/01
2002/0138778	CONTROLLING CPU CORE VOLTAGE TO REDUCE POWER CONSUMPTION	03/22/01

The Examiner's attention is respectfully directed to the following Foreign Patent or Published Foreign Patents:

Document No.	Title	Publication Date
EPO474963	COMPUTER SYSTEM HAVING SLEEP MODE FUNCTION	03/18/92
EPO381021	POWER SAVING SYSTEM	08/08/90
WO01/27728 A1	MINIMIZING POWER CONSUMPTION DURING SLEEP MODES BY USING MINIMUM CORE VOLTAGE NECESSARY TO MAINTAIN SYSTEM STATE	04/19/01

The Examiner's attention is respectfully directed to the following related documents:

Weiser et al.; "SCHEDULING FOR REDUCED CPU ENERGY"; Xerox PARC, Palo Alto, CA; Appears in "Proceedings of the First Symposium on operating Systems Design and Implementation; Usenix Assoc. Nov. 1994

Govil; "COMPARING ALGORITHMS FOR DYNAMIC SPEEDSETTING OF A LOW POWER CPU"; International Computer Science Institute; Berkeley, CA; April 1995

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 3/18/04

By: Ronald M Pomerenke
Ronald M. Pomerenke
Reg. No. 43,009

215 $

Patent

Docket No.: TRAN-P059

Information Disclosure Statement Transmittal

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner of Patents and Trademarks, Washington, D.C., 20231, on the below date of deposit.

Date of Deposit:	03/18/04	Name of Person Making the Deposit:	KATHERINE RINALDI	Signature of the Person Making the Deposit:	Katherine Rinaldi

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Andrew Read, Sameer Halapete and Keith Klayman

Group Art Unit:

Filed: 10/23/00

Examiner:

Serial No.: 09/694,433

Title: STATIC POWER CONTROL

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Information Disclosure Statement Transmittal

Transmitted herewith is the following:

..... Formal drawings, totaling ..... sheets.
..... Informal drawings, totaling ..... sheets.
..... Certification for PTO Consideration
..... Information Disclosure statement (__ sheets)
..X.. Information Disclosure statement and late filing fee
..X.. Form 1449
..... Petition for Extension of Time
..X.. Other: References

Fee Calculation (for other than a small entity)

Fee Items				Fee Rate	Total
Petition for Extension of Time (fee calculated elsewhere				$ .00	$0.00
Information Disclosure Statement, late filing				$180.00	$180.00
Other:					$0.00
Total Fees					$180.00

PAYMENT OF FEES

1. The full fee due in connection with this communication is provided as follows:

[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085 .
A duplicate copy of this authorization is enclosed.

[X] A check in the amount of $180.00

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 3/18/04

By: Ronald M Pomerenke
Ronald M. Pomerenke
Reg. No. 43,009